

Compal Confidential

NAV51 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII

2010-03-31

REV: 1.0

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	Cover Page
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				Date: Tuesday, April 13, 2010	Rev 1.0
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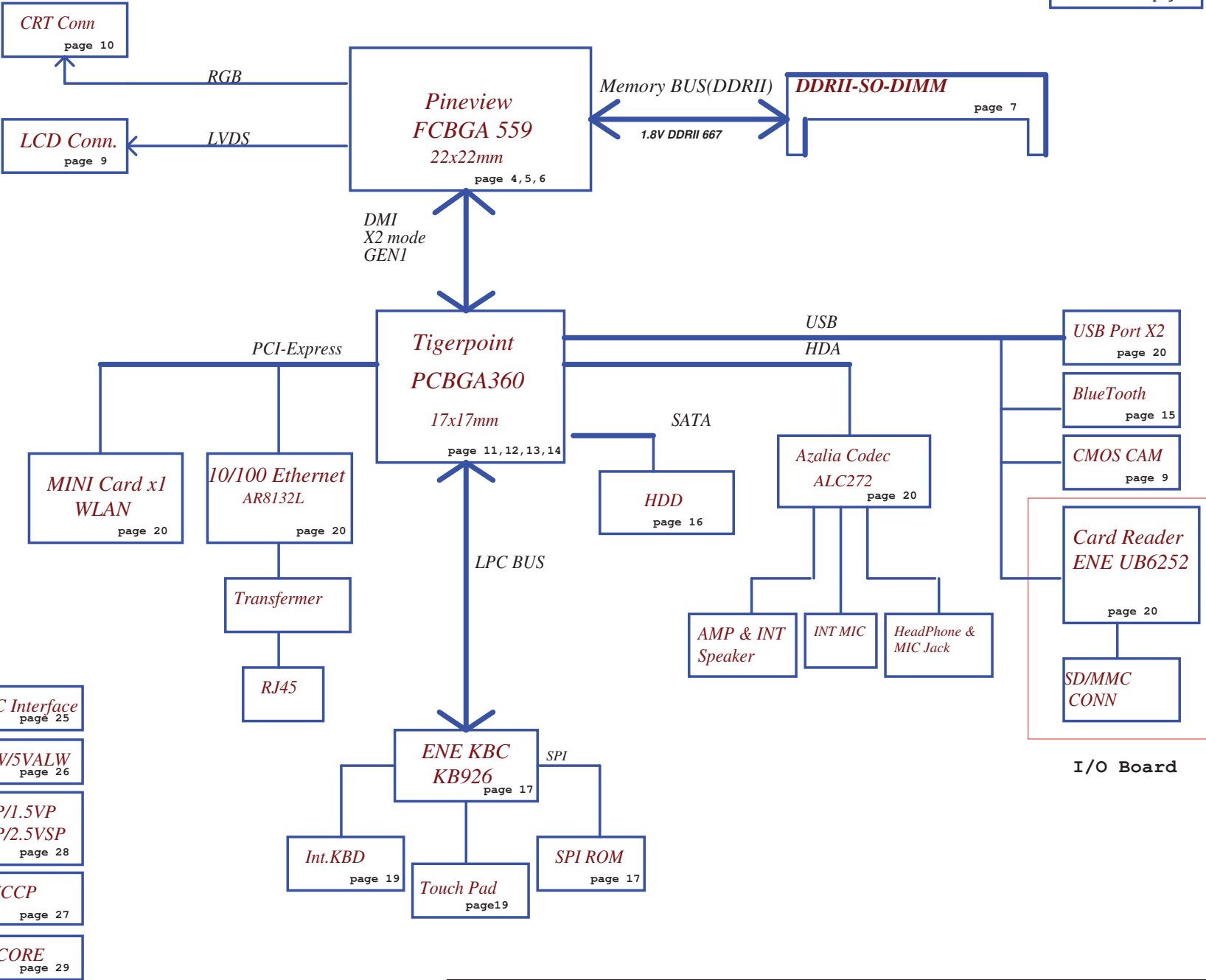
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Model Name : NAV51
File Name : LA-6311P



Clock Generator
CK505
page 8

Thermal Sensor
EMC1402
page 5



Power ON/OFF
page 18

DC IN
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BATT IN
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CHARGER
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CPU_CORE
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DC/DC Interface
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3VALW/5VALW
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0.89VP/1.5VP
0.9VSP/2.5VSP
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1.8V/VCCP
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0 (EVT)	0	0 V	0 V	0 V
1 (DVT)	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2 (PVT)	18K +/- 5%	0.436 V	0.503 V	0.538 V
3 (MP)	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCE Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

EC SM Bus2 address

Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

USB table

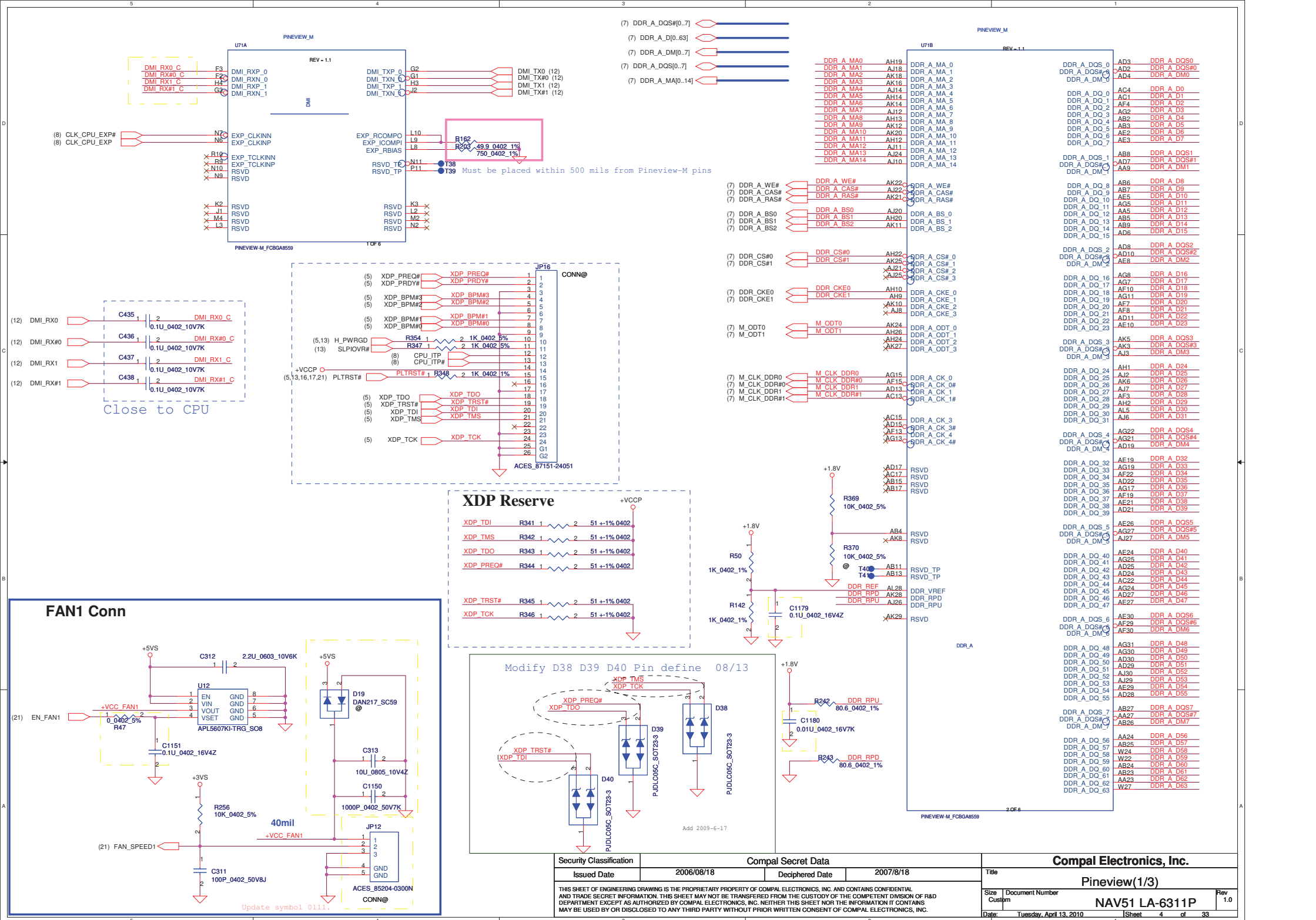
EHCI1	UHCI1	Port0	MB USB Conn1.
		Port1	MB USB Conn2.
	UHCI2	Port2	
		Port3	CMOS
EHCI2	UHCI3	Port4	Card Reader
		Port5	
	UHCI4	Port6	BT
		Port7	WLAN
	UHCI5	Port8	
		Port9	
	UHCI6	Port10	
		Port11	

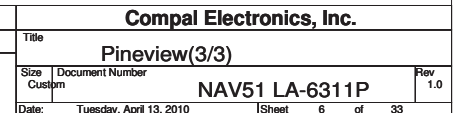
PCIE table

PCIE port1	LAN
PCIE port2	Wireless Card
PCIE port3	
PCIE port4	
PCIE port5	
PCIE port6	

SATA table

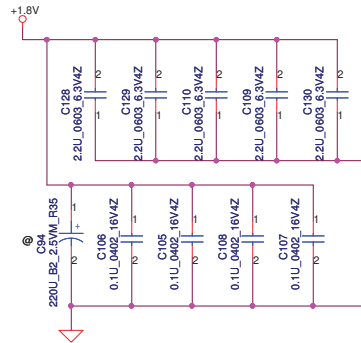
SATA port0	HDD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	



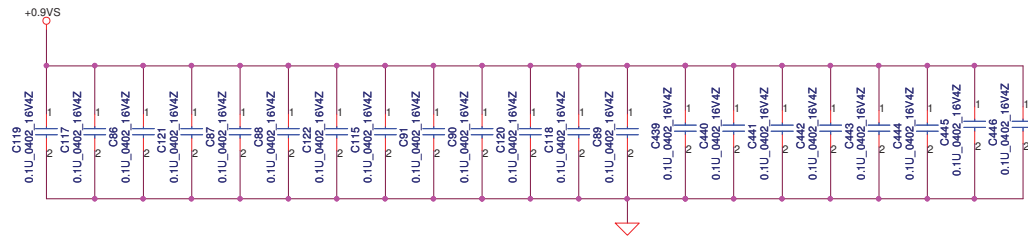


- (4) DDR_A_DQS#0..7
- (4) DDR_A_D[0..63]
- (4) DDR_A_DM0..7
- (4) DDR_A_DQS0..7
- (4) DDR_A_MA[0..14]

Layout Note:
Place near JDIM1

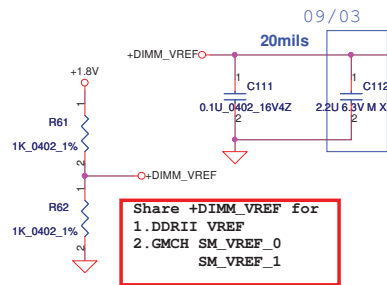


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely DIMMA, all
trace length < 1000 mil

Layout Note:
Place these resistor
closely DIMMA, all
trace length
Max=1000 mil

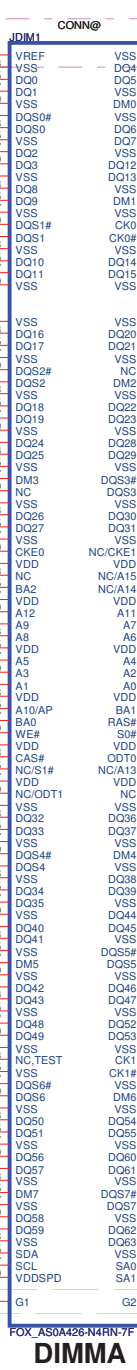
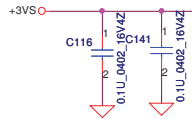


Share +DIMM_VREF for
1. DDRII VREF
2. GMCH SM_VREF_0
SM_VREF_1

- (4) DDR_CKE0
- (4) DDR_A_BS2
- (4) DDR_A_BS0
- (4) DDR_A_WE#
- (4) DDR_A_CAS#
- (4) DDR_CS#1
- (4) M_ODT1

- DDR_CKE0
- DDR_A_BS2
- DDR_A_MA12
- DDR_A_MA9
- DDR_A_MA8
- DDR_A_MA5
- DDR_A_MA3
- DDR_A_MA1
- DDR_A_MA10
- DDR_A_BS0
- DDR_A_WE#
- DDR_A_CAS#
- DDR_CS#1
- M_ODT1
- DDR_A_D32
- DDR_A_D33
- DDR_A_DQS#4
- DDR_A_DQS4
- DDR_A_D34
- DDR_A_D35
- DDR_A_D40
- DDR_A_D41
- DDR_A_DM5
- DDR_A_D42
- DDR_A_D43
- DDR_A_D48
- DDR_A_D49
- DDR_A_DQS#6
- DDR_A_DQS6
- DDR_A_D50
- DDR_A_D51
- DDR_A_D56
- DDR_A_D57
- DDR_A_DM7
- DDR_A_D58
- DDR_A_D59

- (8,17) CLK_SMBDATA
- (8,17) CLK_SMBCLK



DIMMA

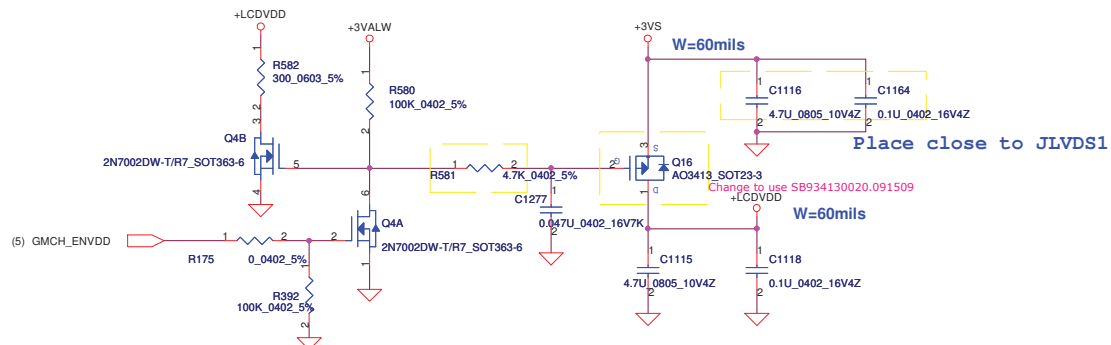
Change to SP07F001720 04/30

- DDR_A_D4
- DDR_A_D5
- DDR_A_DM0
- DDR_A_D6
- DDR_A_D7
- DDR_A_D12
- DDR_A_D13
- DDR_A_DM1
- M_CLK_DDR0
- M_CLK_DDR#0
- DDR_A_D14
- DDR_A_D15
- DDR_A_D20
- DDR_A_D21
- DDR_A_DM2
- DDR_A_D22
- DDR_A_D23
- DDR_A_D28
- DDR_A_D29
- DDR_A_DQS#3
- DDR_A_DQS3
- DDR_A_D30
- DDR_A_D31
- DDR_CKE1
- DDR_A_MA14
- DDR_A_MA11
- DDR_A_MA7
- DDR_A_MA6
- DDR_A_MA4
- DDR_A_MA2
- DDR_A_MA0
- DDR_A_BS1
- DDR_A_RAS#
- DDR_CS#0
- M_ODT0
- DDR_A_MA13
- DDR_A_D36
- DDR_A_D37
- DDR_A_DM4
- DDR_A_D38
- DDR_A_D39
- DDR_A_D44
- DDR_A_D45
- DDR_A_DQS#5
- DDR_A_DQS5
- DDR_A_D46
- DDR_A_D47
- DDR_A_D52
- DDR_A_D53
- M_CLK_DDR1
- M_CLK_DDR#1
- DDR_A_DM6
- DDR_A_D54
- DDR_A_D55
- DDR_A_D60
- DDR_A_D61
- DDR_A_DQS#7
- DDR_A_DQS7
- DDR_A_D62
- DDR_A_D63

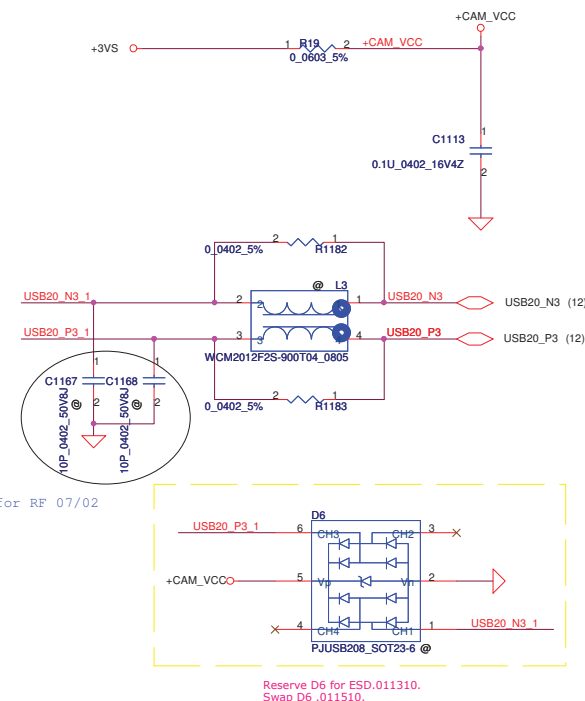
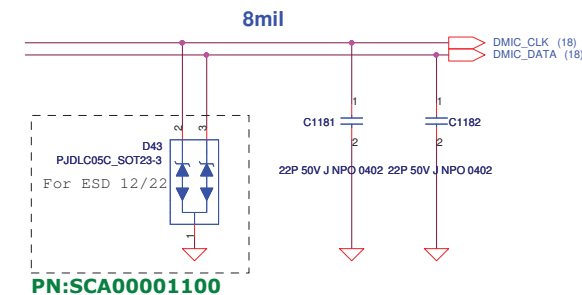
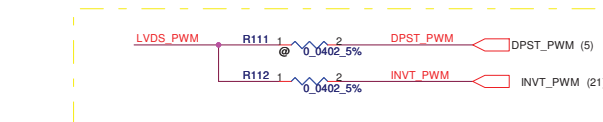
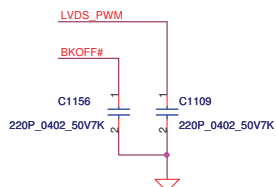
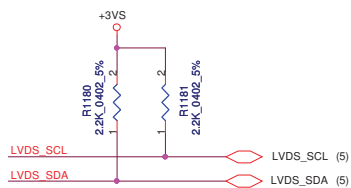
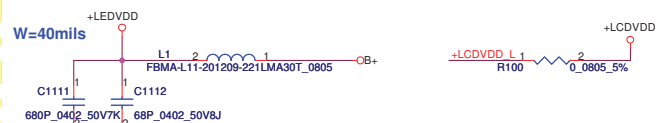
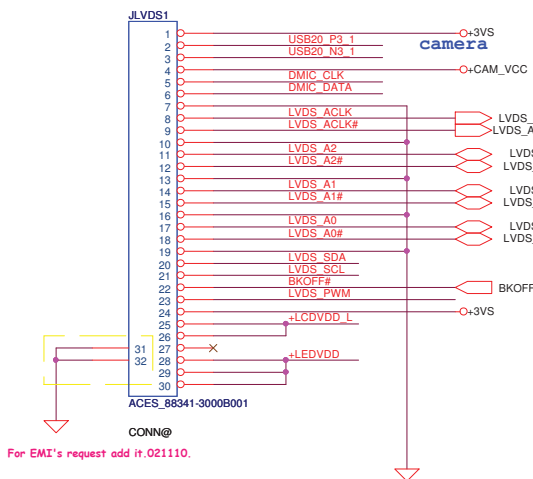
For EMI's request add it.021110.

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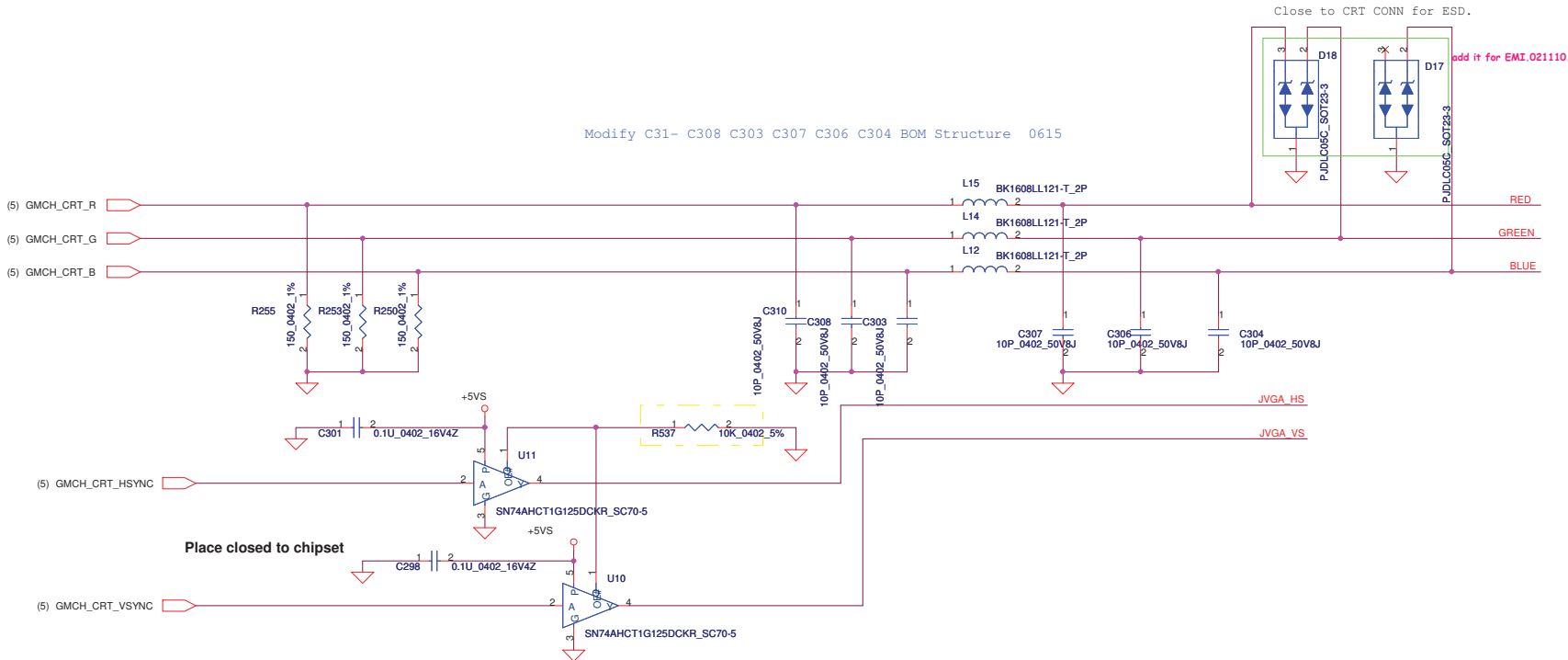
LCD POWER CIRCUIT



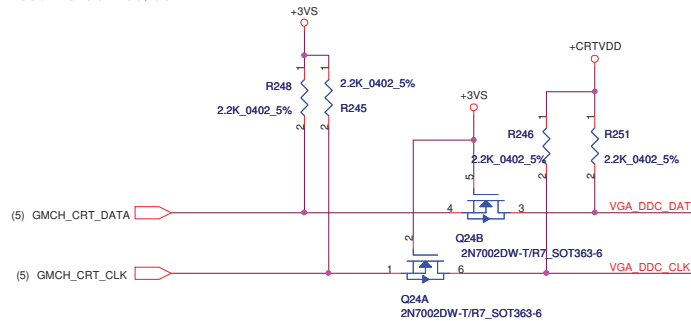
CMOS & LCD/PANEL BD. Conn.



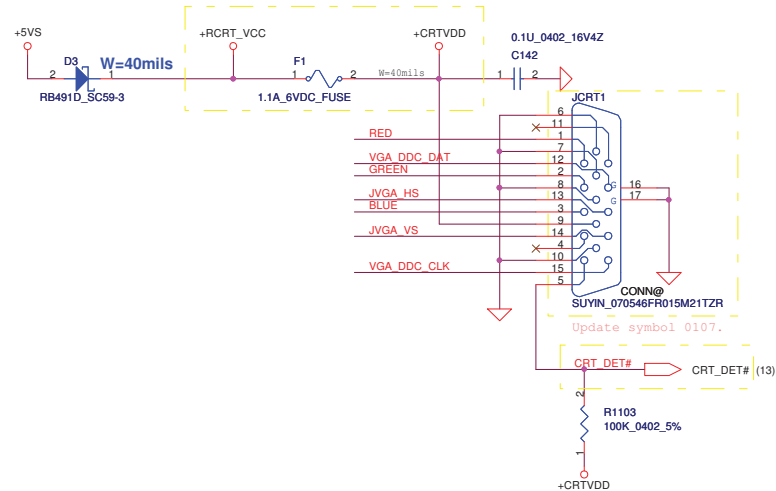
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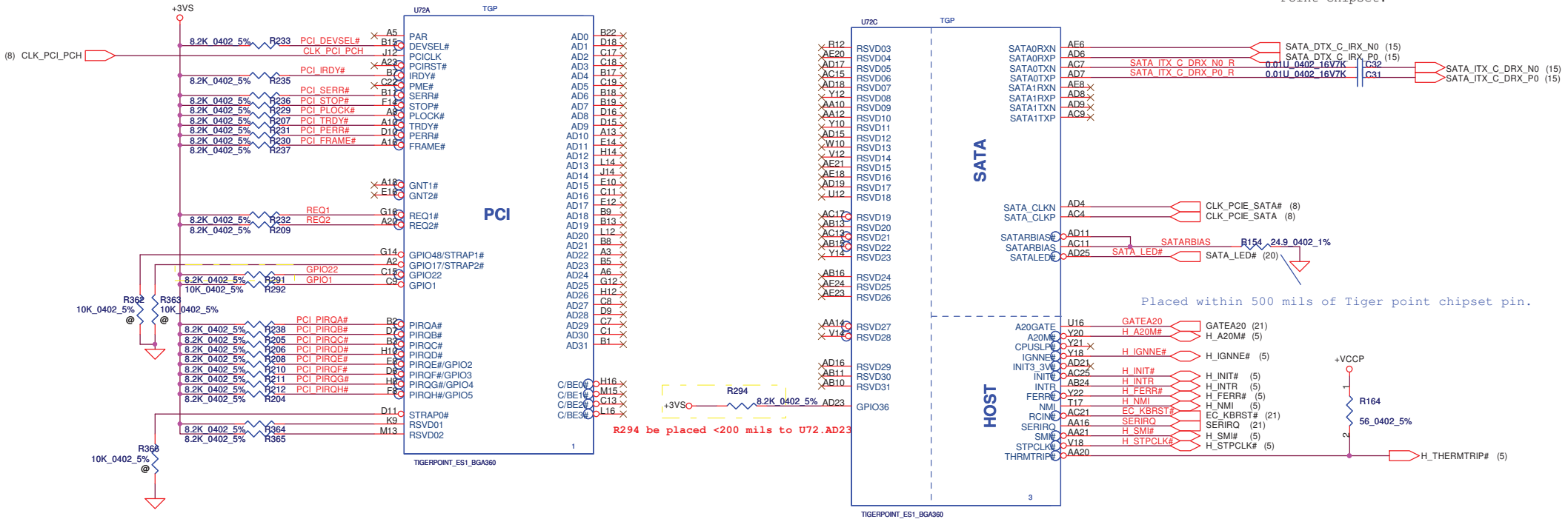
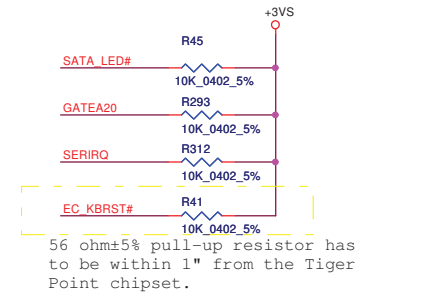
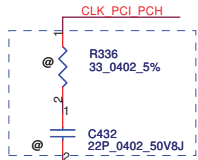
Add R1283 R1284
Change R247 R249 to 10 ohm
Add @ on U10 U11 C301 C298 06/08



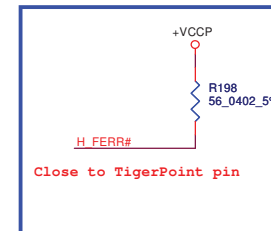
CRT PORT



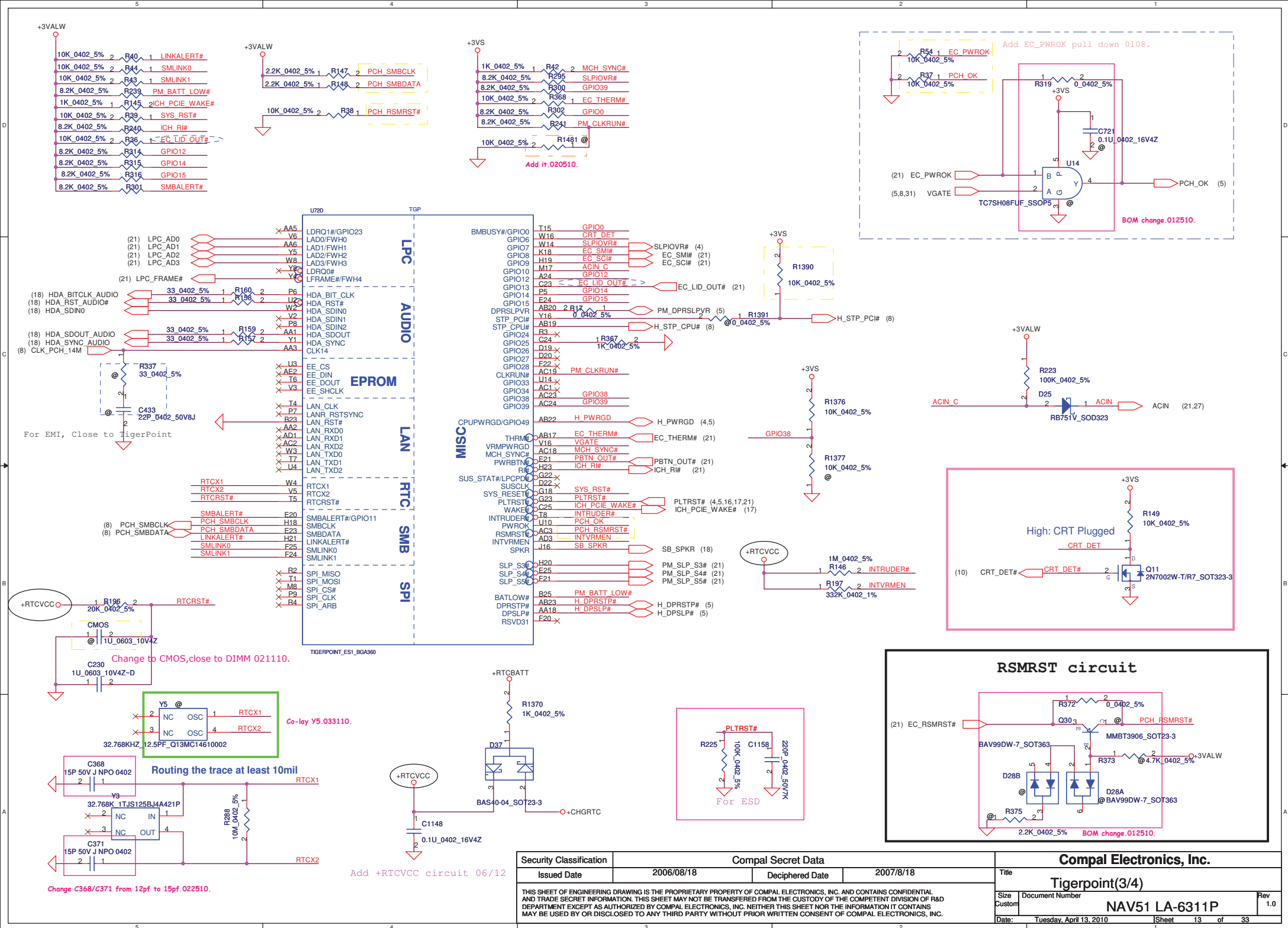
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								CRT PORT							
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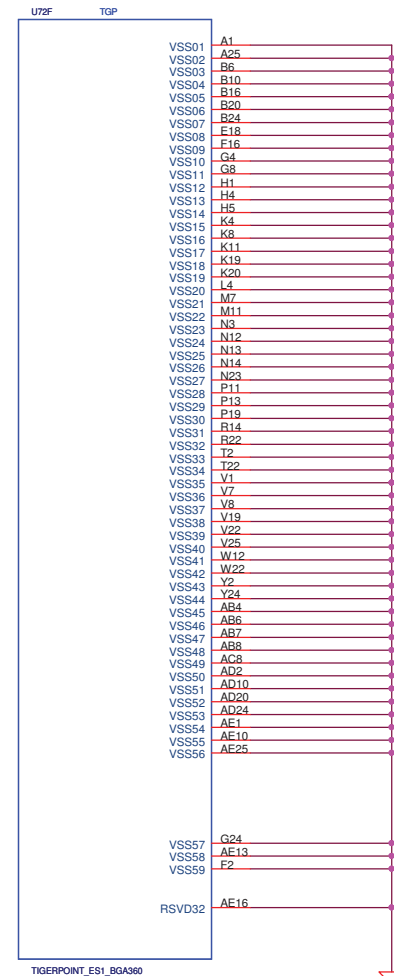
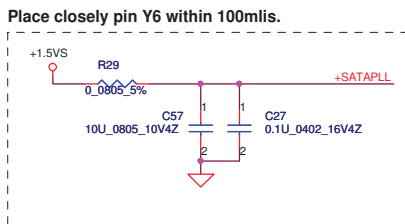
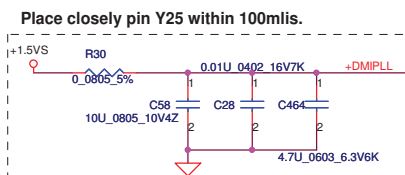
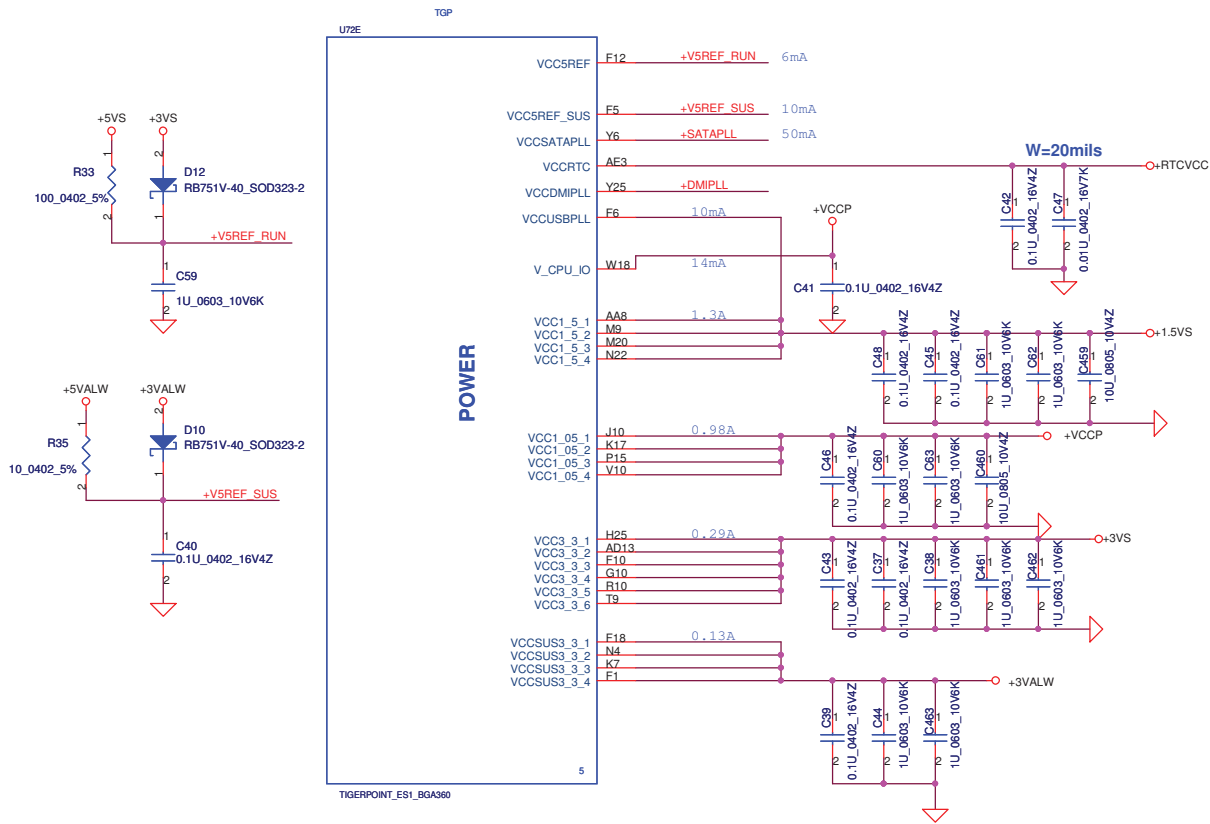


STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC



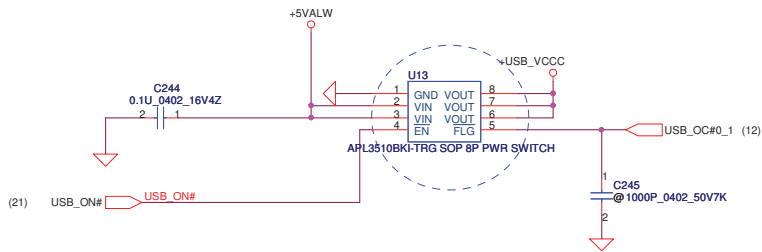
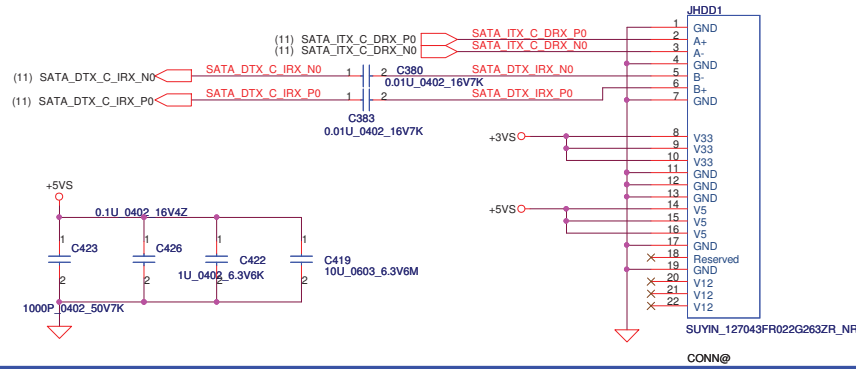
ESD request		
H_A20M#	C450@	2 100P 0402 50V8J
H_IGNNE#	C451@	2 100P 0402 50V8J
H_INIT#	C452@	2 100P 0402 50V8J
H_INTR	C453@	2 100P 0402 50V8J
H_FERR#	C454@	2 100P 0402 50V8J
H_NMI	C455@	2 100P 0402 50V8J
H_SMI#	C456@	2 100P 0402 50V8J
H_STPCLK#	C457@	2 100P 0402 50V8J



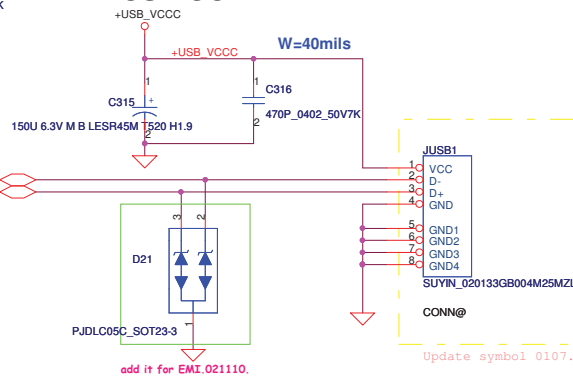


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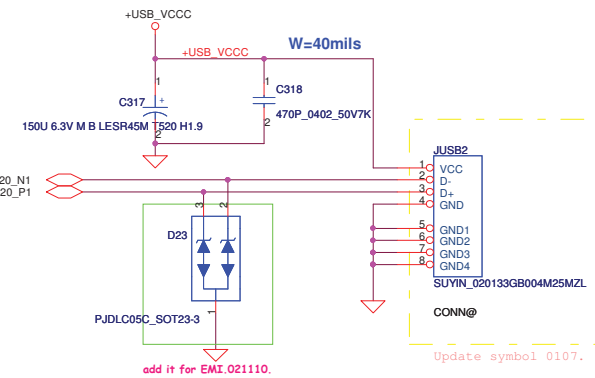
SATA HDD Conn.



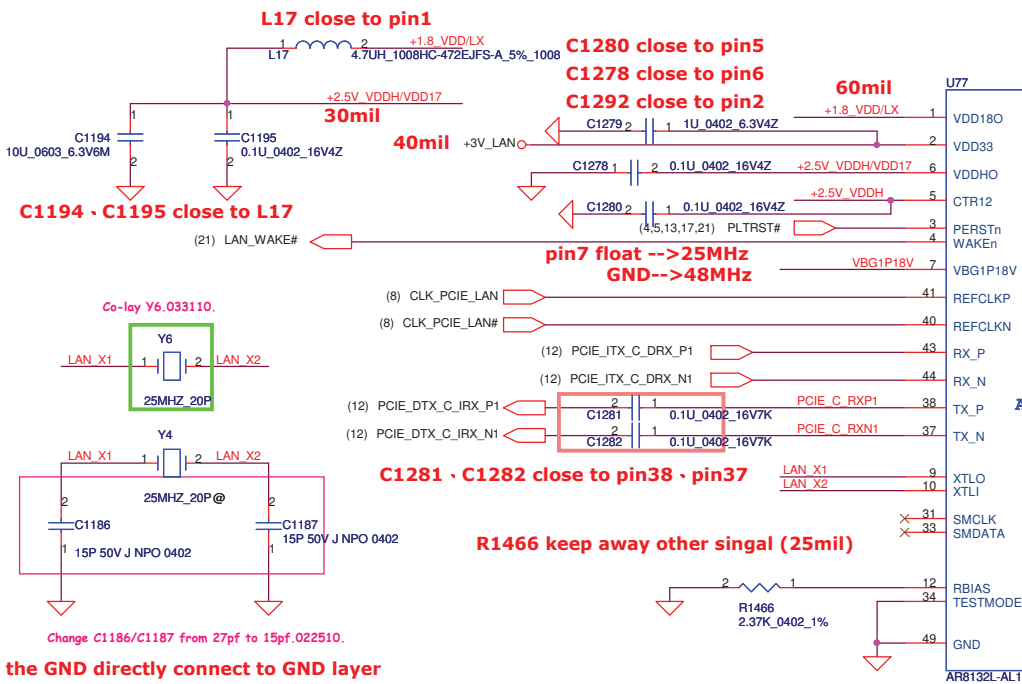
USB CONN.1



USB CONN.2



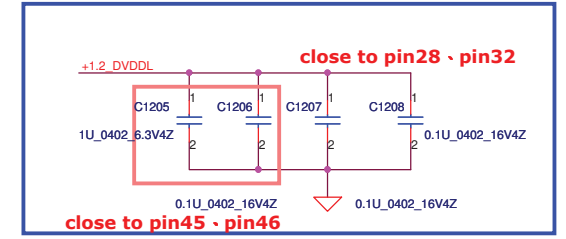
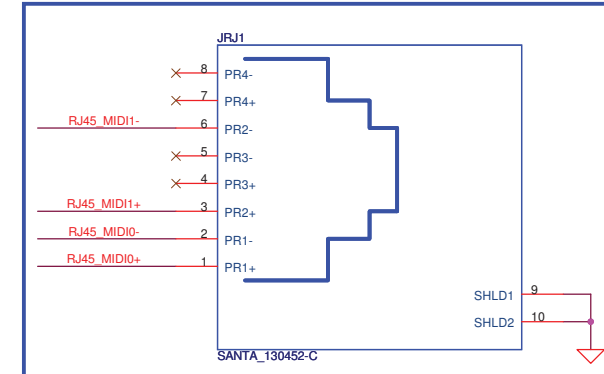
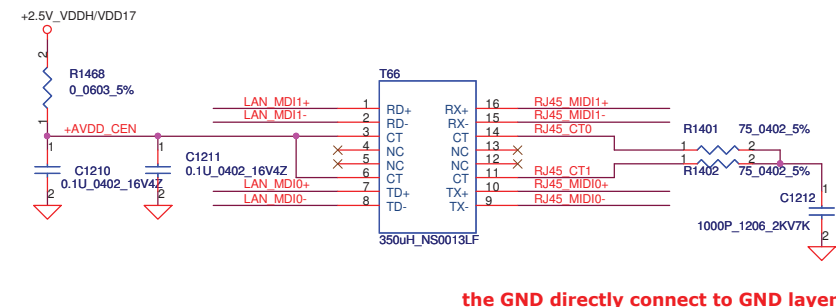
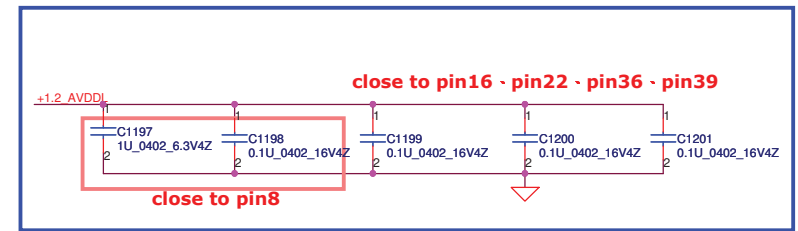
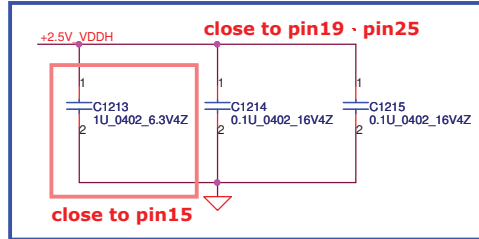
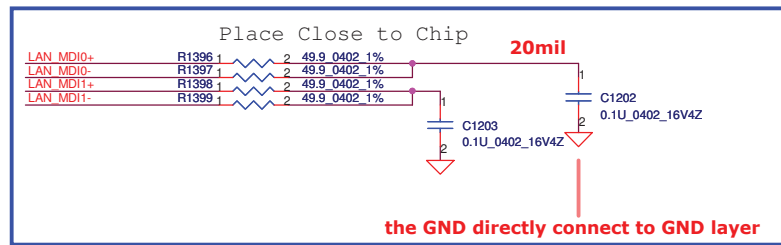
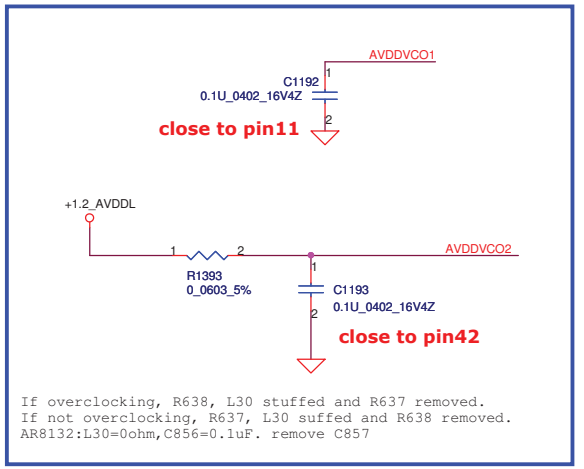
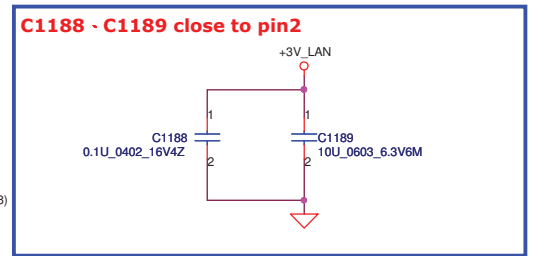
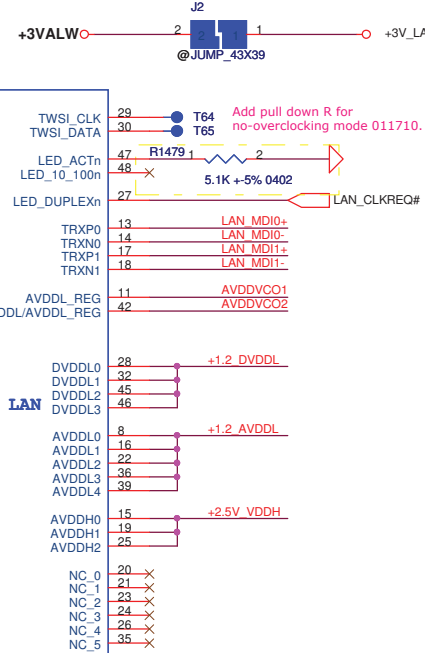
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Atheros

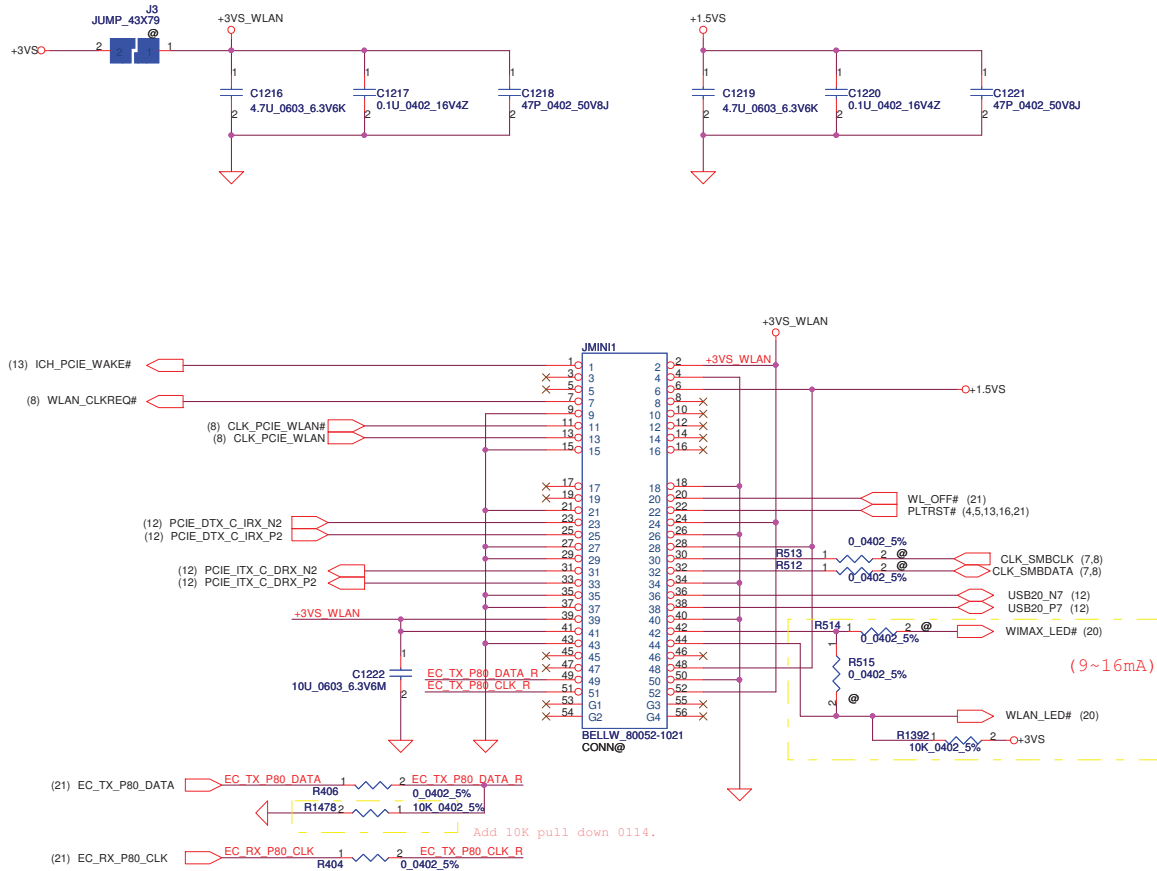
AR8114A 10/100 LAN

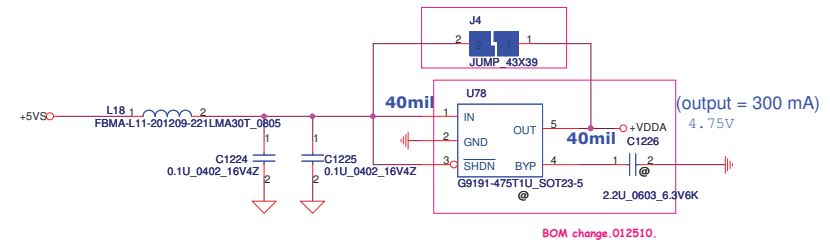
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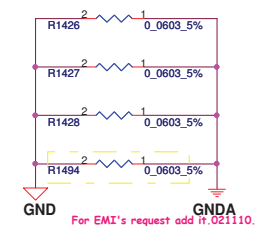
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Mini-Express Card for WLAN



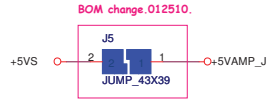


HD Audio Codec



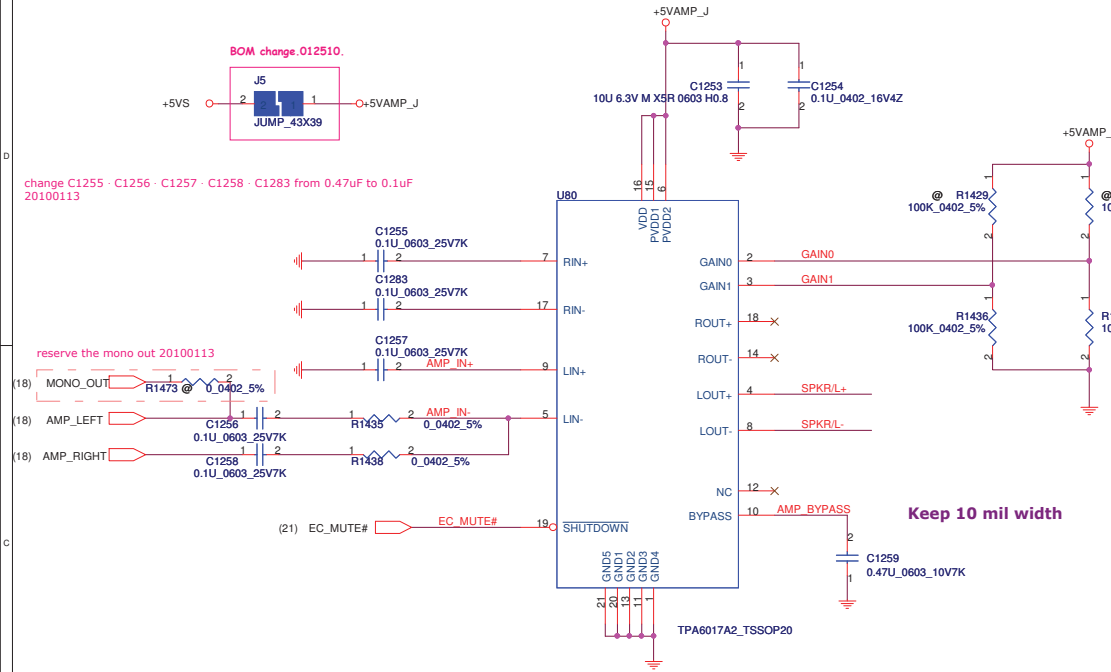
Change to SA00002CI20 ALC272-VA2-GR

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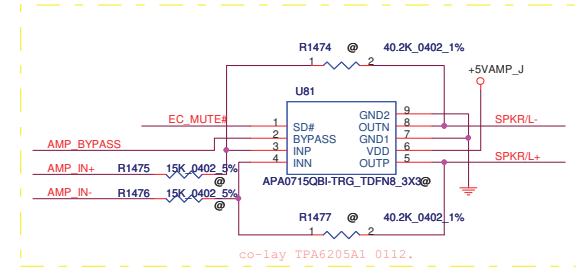
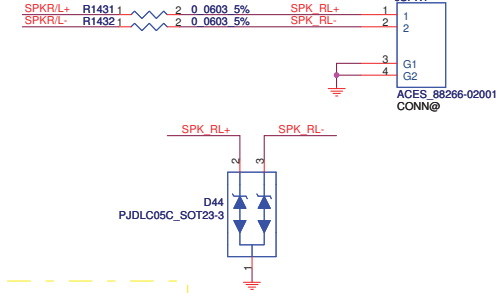
change C1255 · C1256 · C1257 · C1258 · C1283 from 0.47uF to 0.1uF 20100113

reserve the mono out 20100113

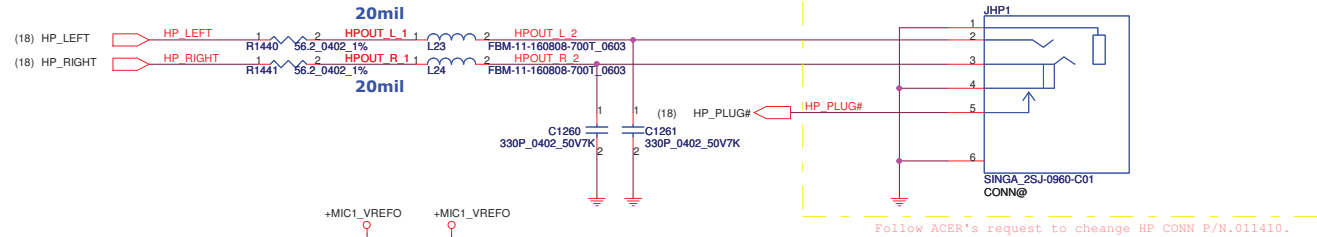


Int. Speaker Conn.

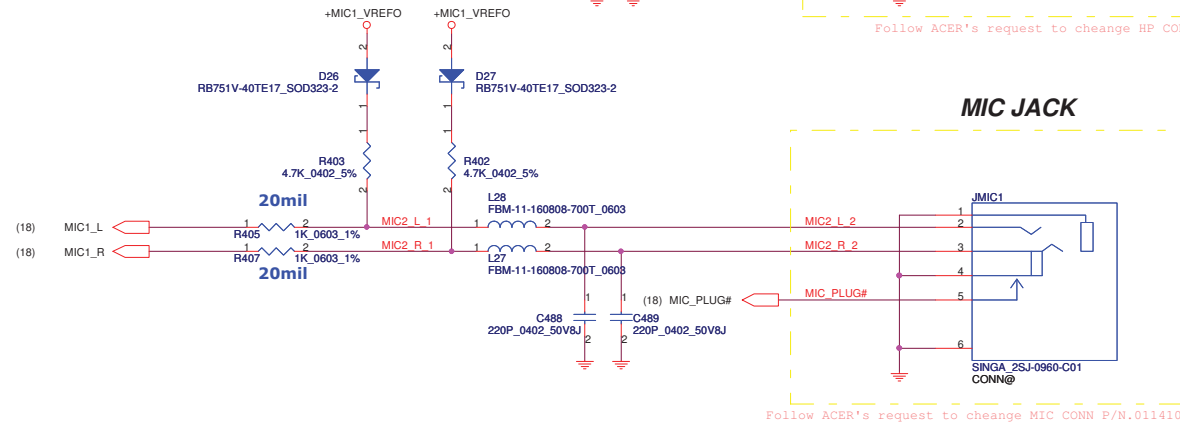
20mil



(Use NAL00 PCB Footprint) Headphone Out



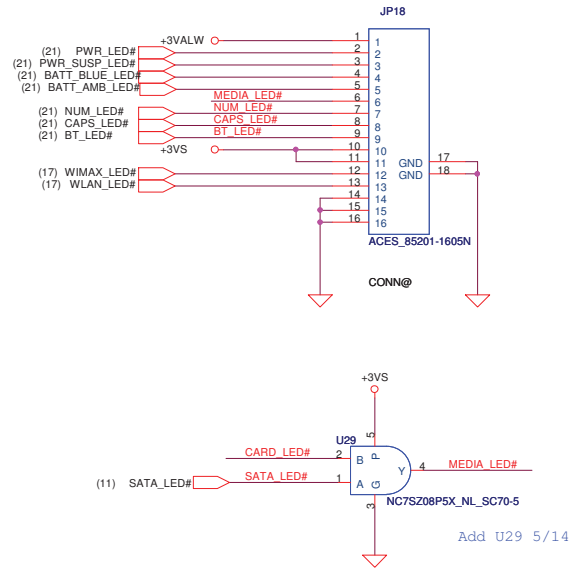
MIC JACK



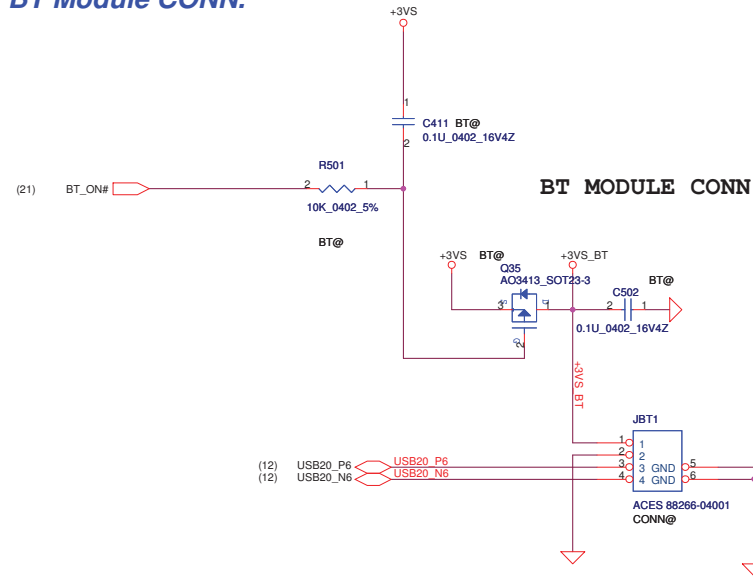
Compal Electronics, Inc.

Title	<Title> Amplifier & Audio Jack		
Size	Document Number	Rev	0.1
Custom	NAV51 LA-6311P	NAV51 LA-6311P	
Date:	Tuesday, April 13, 2010	Sheet	19 of 33

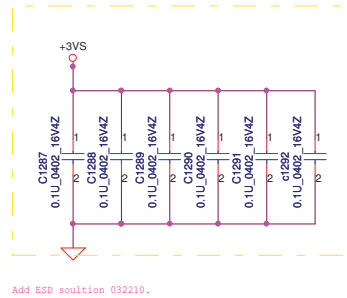
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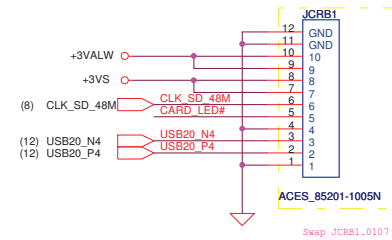
BT Module CONN.



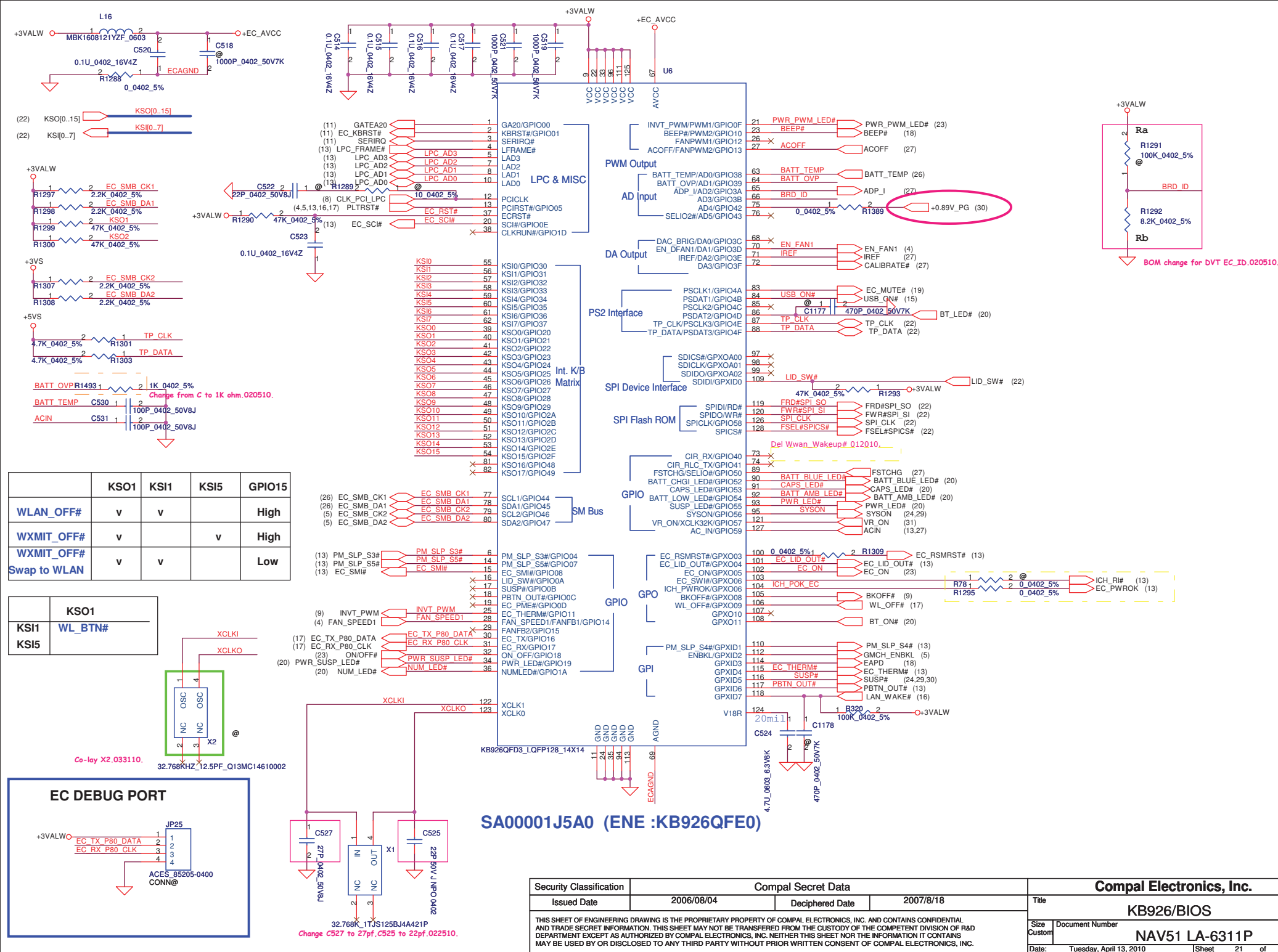
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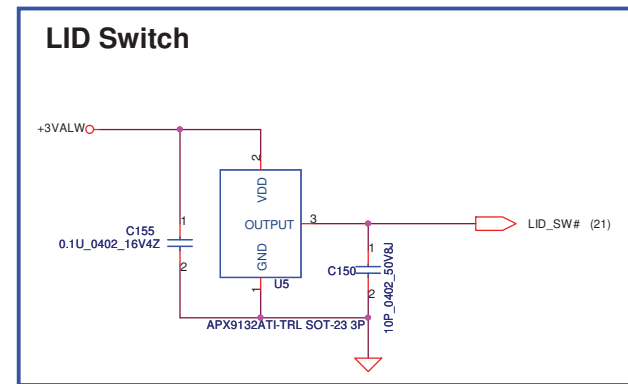
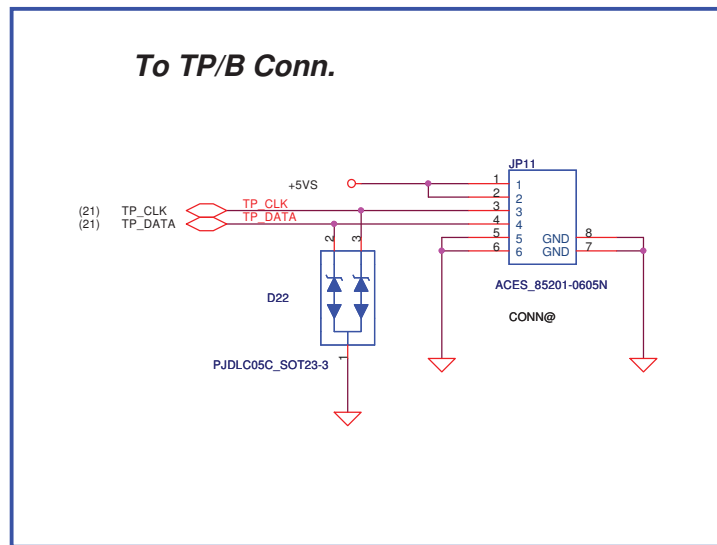
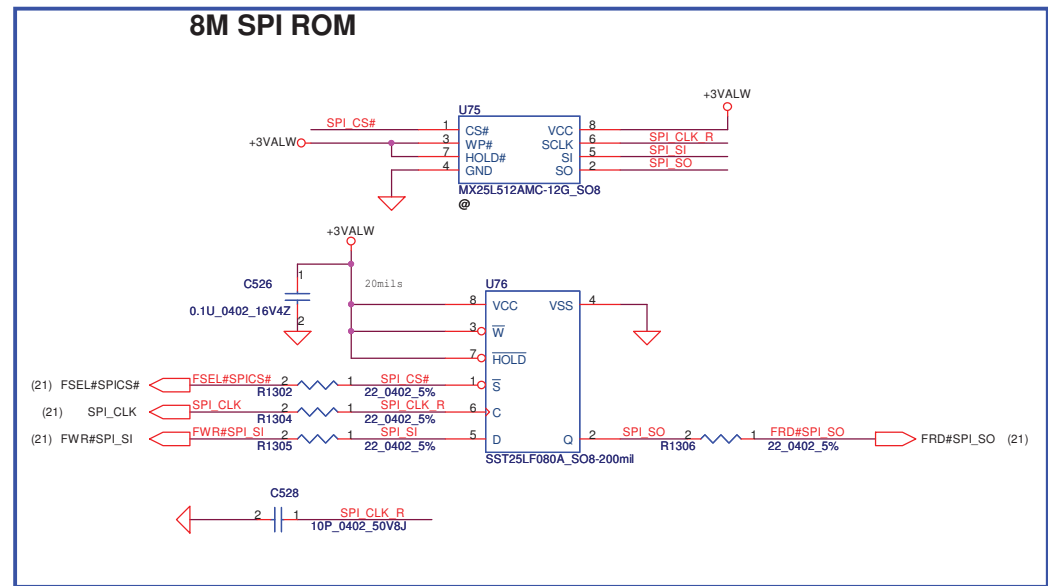
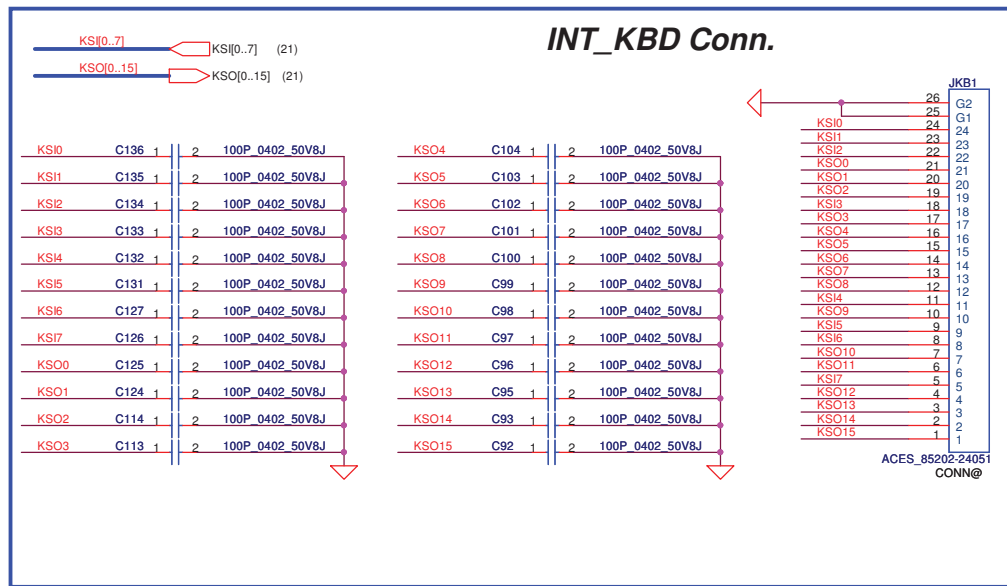
Card Reader CONN.



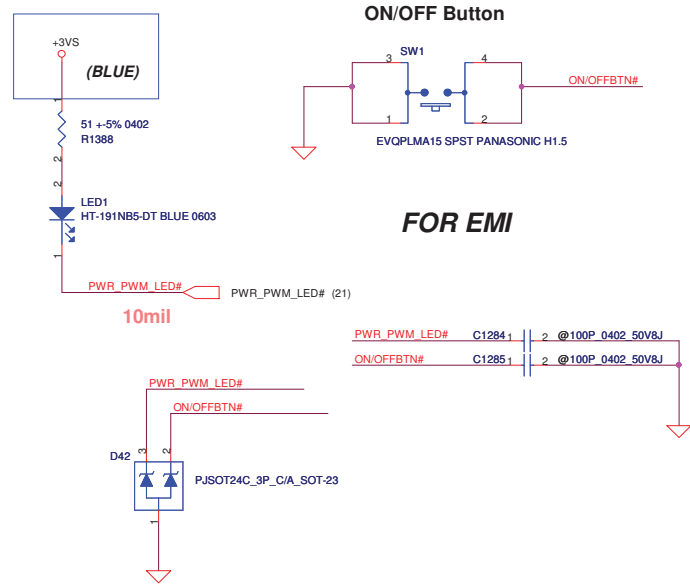
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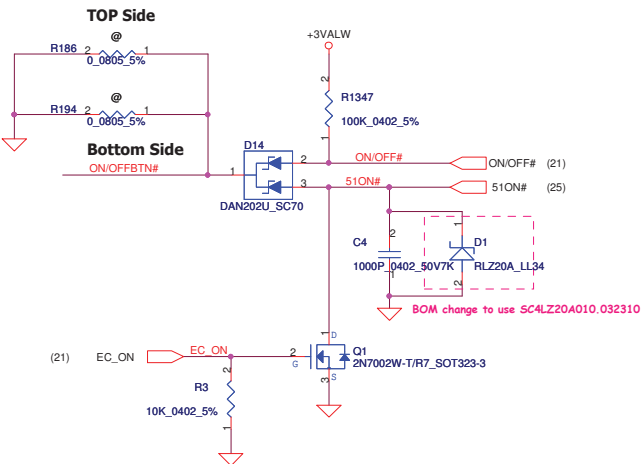
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Add For NAV50 07/06
09/03 Change +5VS to +3VS



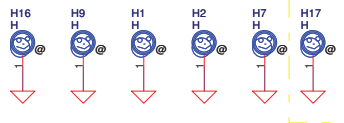
Power Button Logic



H_3P2X3P7N



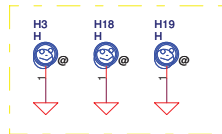
H_2P6



H_3P0



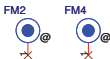
H_3P3



H_3P3N



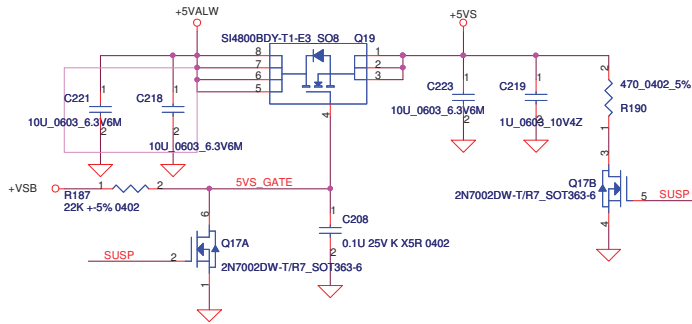
H_3P4X3P2N



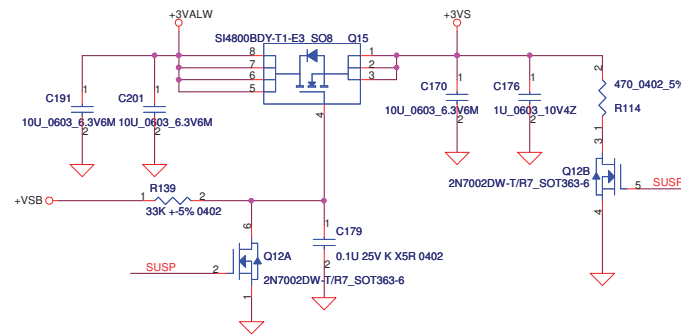
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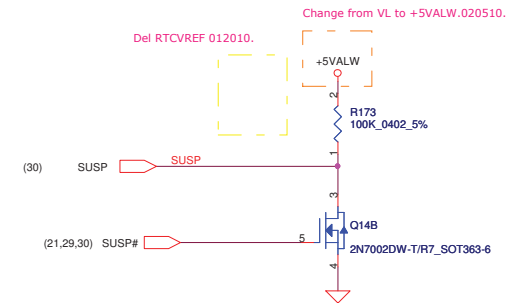
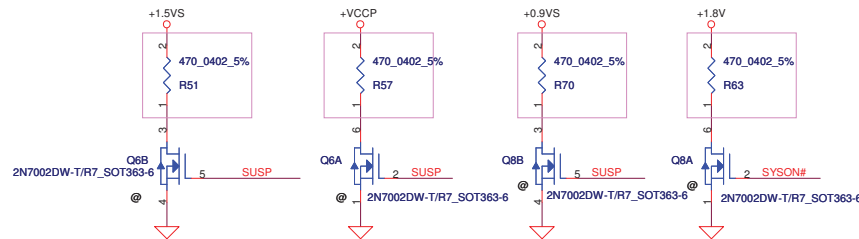
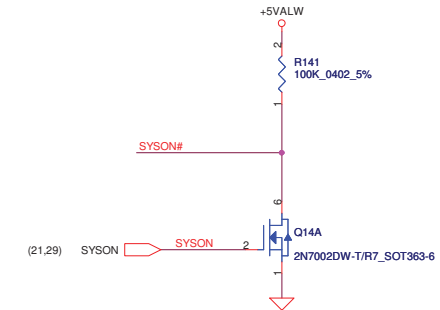
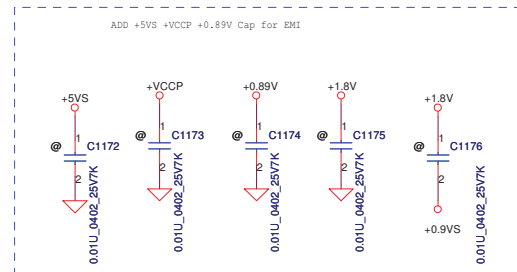
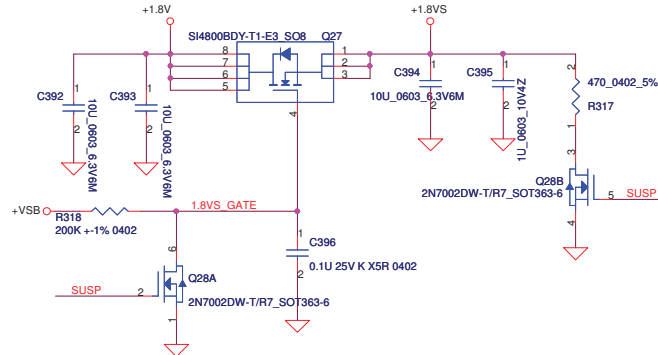
+5VALW TO +5VS



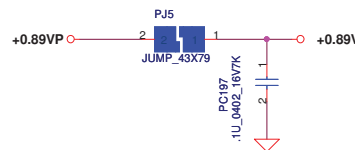
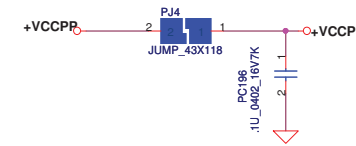
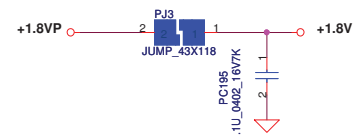
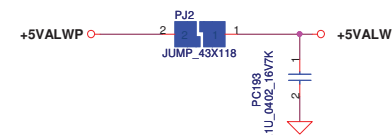
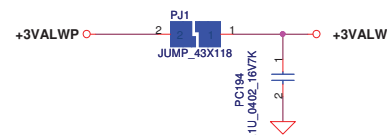
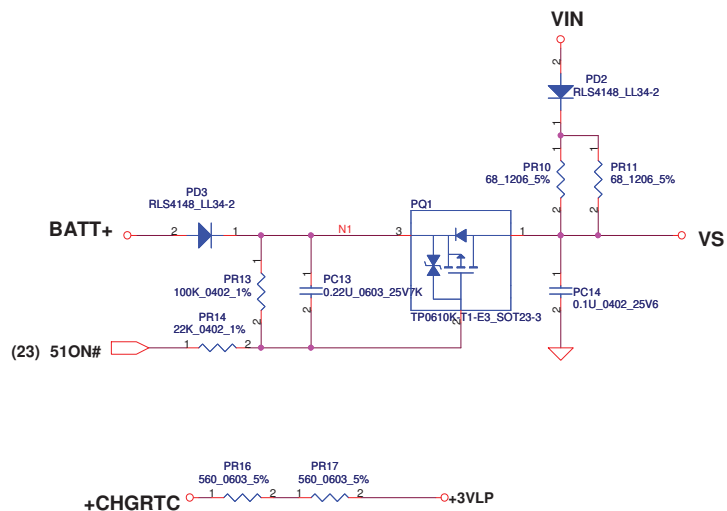
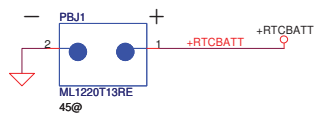
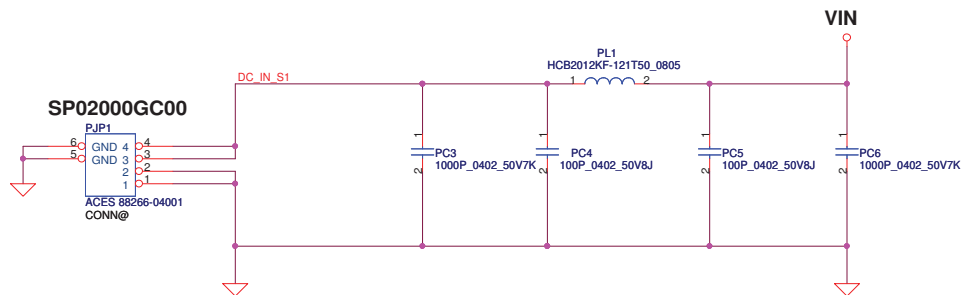
+3VALW TO +3VS



+1.8V to +1.8VS

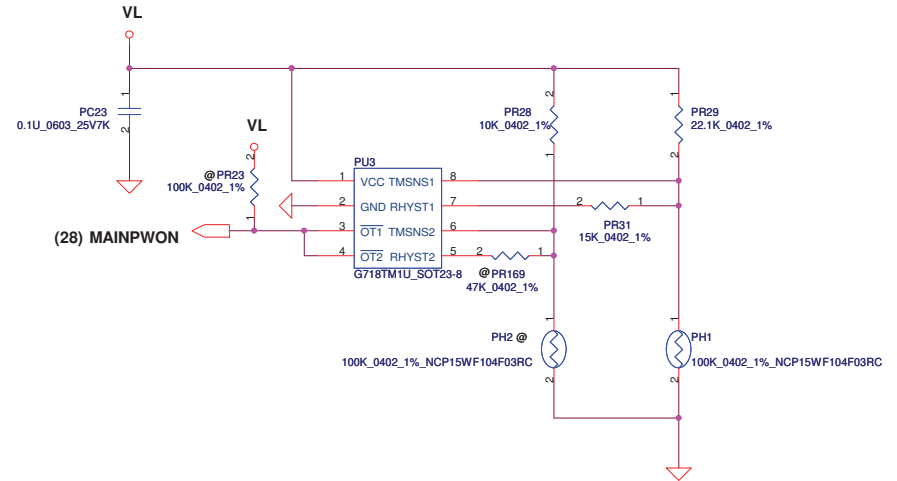
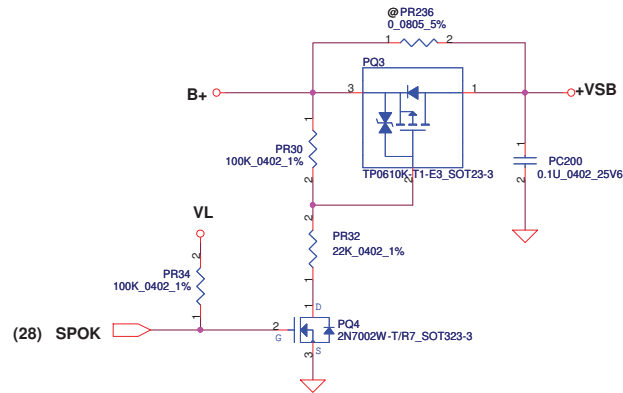
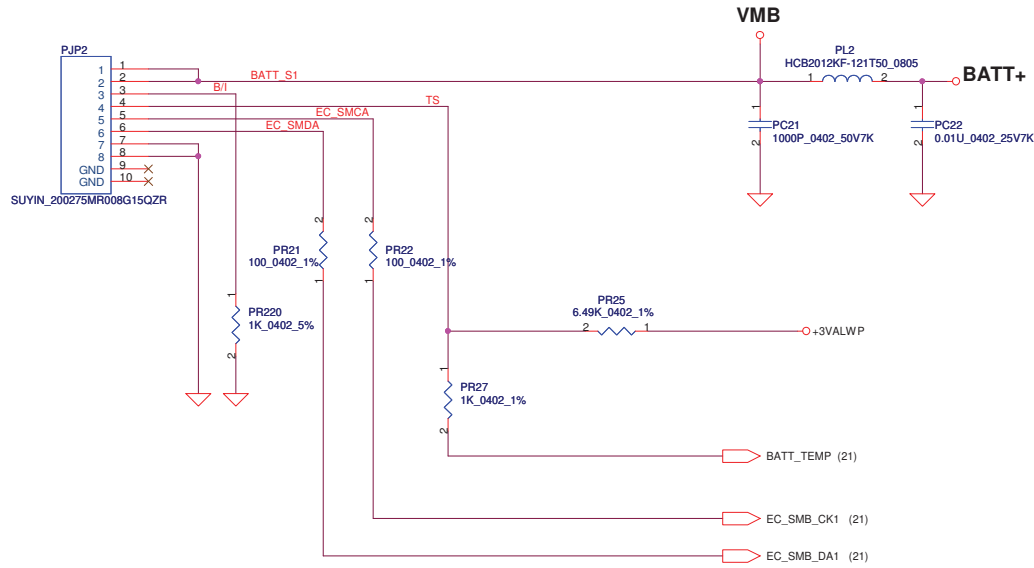


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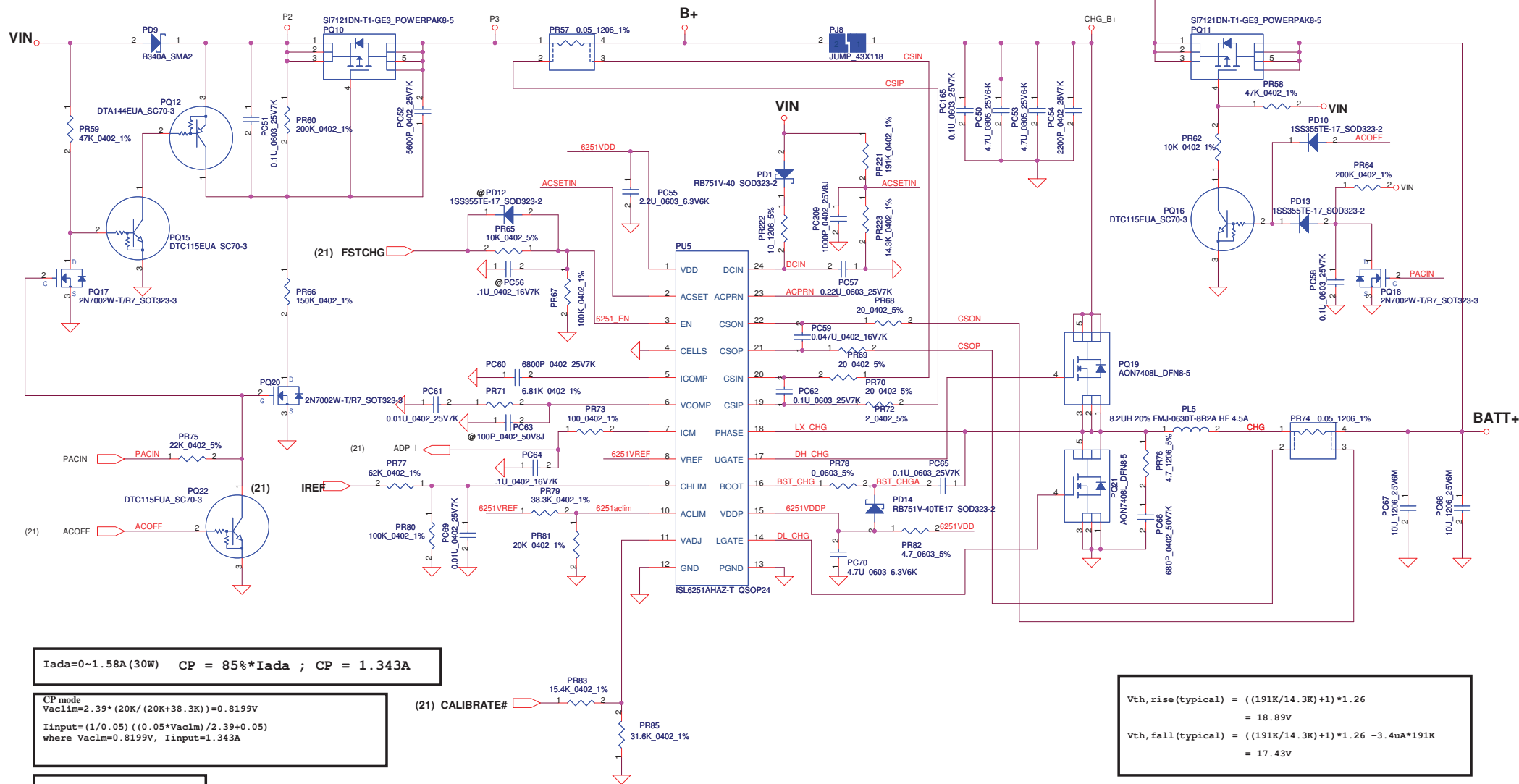


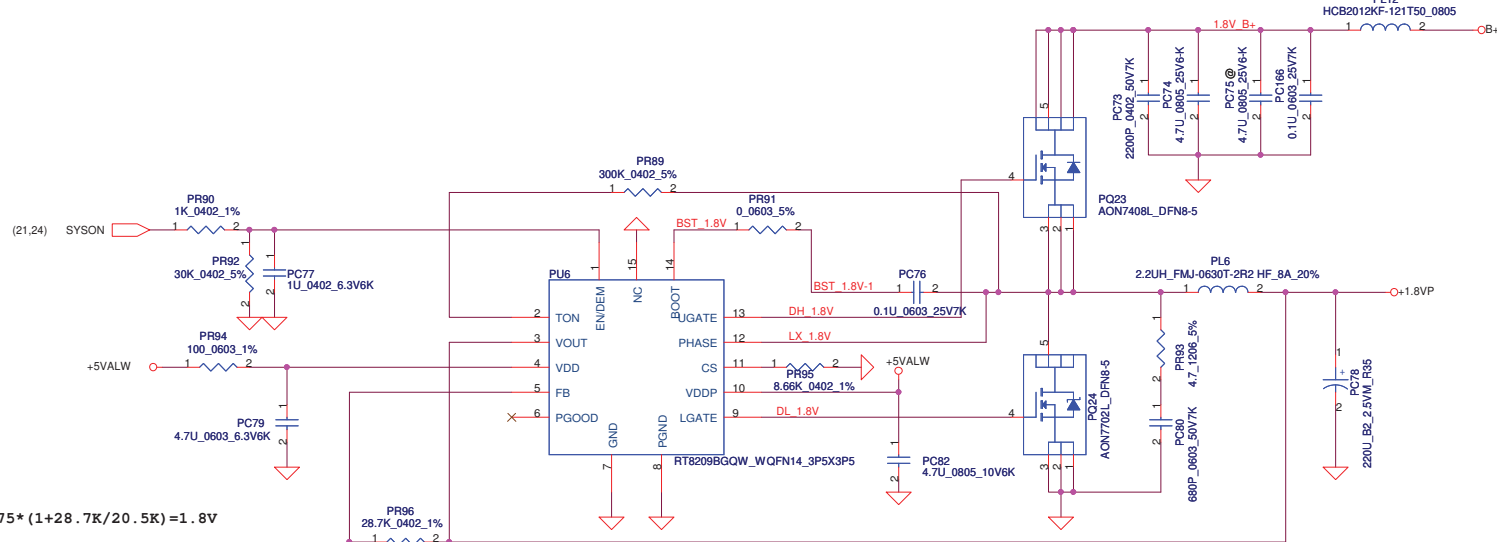
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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C

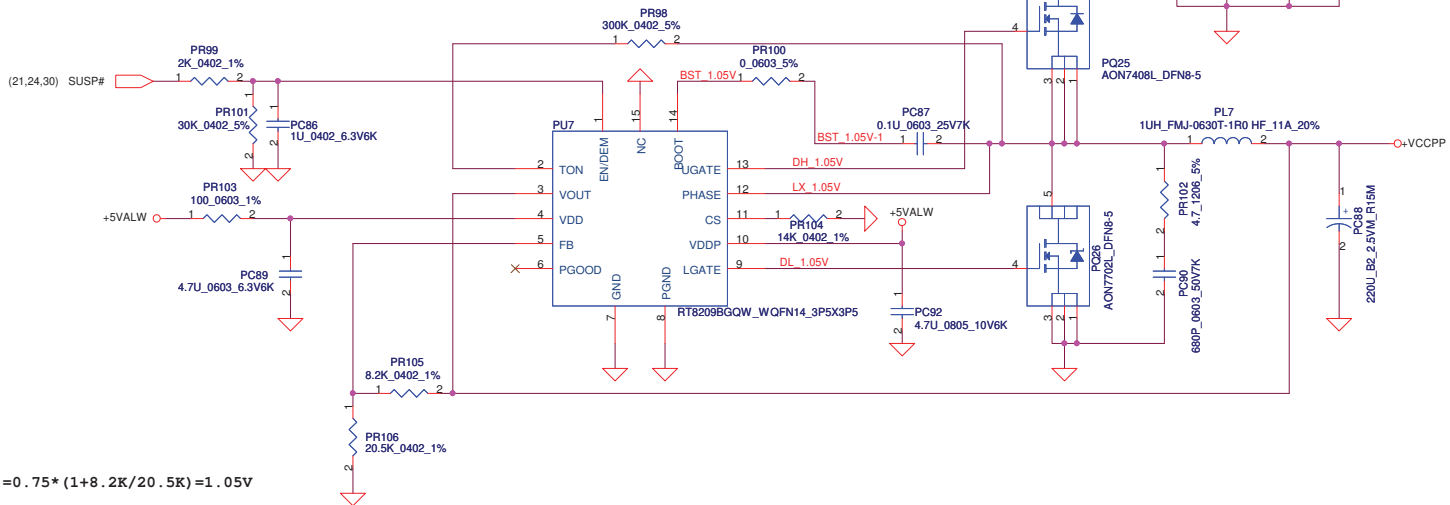


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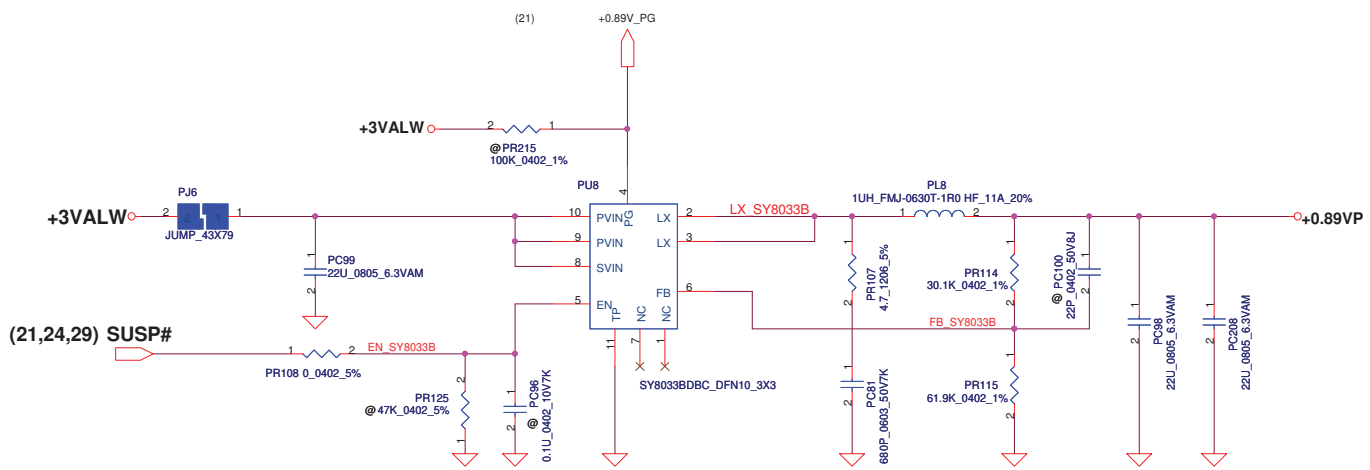


$V_o = 1.8V$ $V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR96/PR97) = 0.75 * (1 + 28.7K/20.5K) = 1.8V$
 $F_{sw} = 328KHz$
 $C_{out} ESR = 15m\ \Omega$ $R_{dson(max)} = 17.9m\ \Omega$ $R_{dson(typical)} = 14.5m\ \Omega$
 $I_{peak} = 4.97A$, $I_{max} = 3.479A$, $I_{ocp} = 5.964A$
 $\Delta I = ((19 - 1.8) * (1.8/19)) / (2.2u * 328K) = 2.259A$
 $\Rightarrow 1/2 \Delta I = 1.129A$
 $V_{trip} = R_{trip} * I_{ocp} = 8.66K * 10uA = 0.0866V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.129$
 $= 0.0866 / (0.0179) + 1.129 = 5.967A$
 $I_{ocpmax} = (0.0866 / (0.0145 * 1.2)) + 1.129A = 6.106A$
 $I_{ocp} = 5.967A \sim 6.106A$

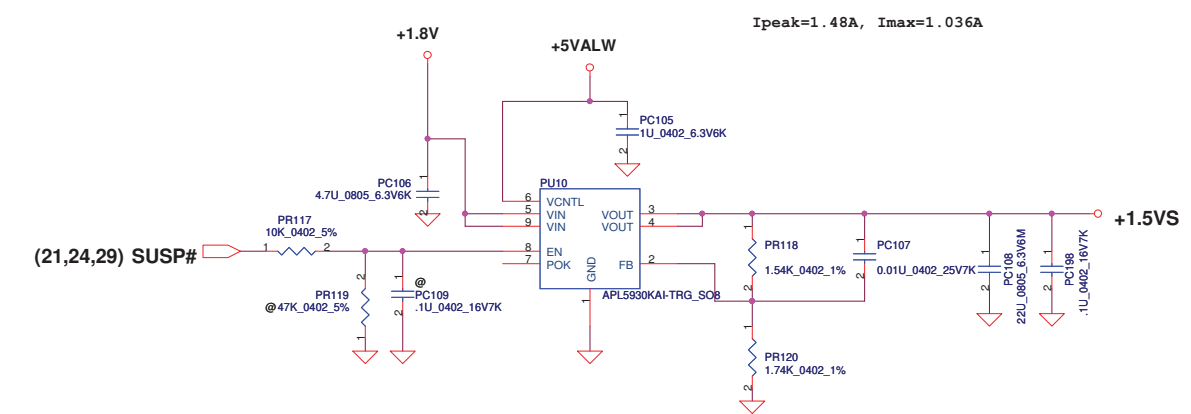


$V_o = 1.05V$ $V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR105/PR106) = 0.75 * (1 + 8.2K/20.5K) = 1.05V$
 $F_{sw} = 280KHz$
 $C_{out} ESR = 15m\ \Omega$ $R_{dson(max)} = 17.9m\ \Omega$ $R_{dson(typical)} = 14.5m\ \Omega$
 $I_{peak} = 3.124A$, $I_{max} = 2.187A$, $I_{ocp} = 3.749A$
 $\Delta I = ((19 - 1.05) * (1.05/19)) / (1.5u * 280K) = 3.549A$
 $\Rightarrow 1/2 \Delta I = 1.774A$
 $V_{trip} = R_{trip} * I_{ocp} = 14K * 10uA = 0.14V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.774$
 $= 0.14 / (0.0179) + 1.774 = 9.596A$
 $I_{ocpmax} = (0.14 / (0.0145 * 1.2)) + 1.774A = 9.820A$
 $I_{ocp} = 9.596A \sim 9.820A$

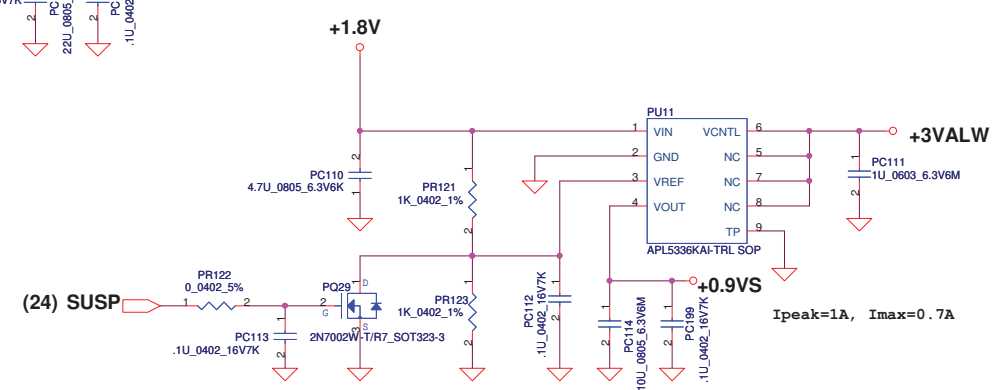
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$V_o = 0.89V$ $V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR114 / PR115) = 0.6 * (1 + 30.1K / 61.9) = 0.89V$
 $I_{peak} = 2.64A$, $I_{max} = 1.848A$



$I_{peak} = 1.48A$, $I_{max} = 1.036A$



$I_{peak} = 1A$, $I_{max} = 0.7A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						2010.1.8	EVT
2						2010.1.11	EVT
3							
4							
5							
6							
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				PIR_HW	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	PU8 Vin change to +3VALW	modify for HW layout request	0.1	30		2010.1.8	EVT
2	PU4 Pin25 change to no connect	modify for 3/5V load balance(TI FAE request)	0.1	28		2010.1.11	EVT
3							
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